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09/465,634	12/17/1999	DAVID K. VAVRO	INTL-0286-US	9115

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/465,634	Applicant(s) VAVRO ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8-10, 14, 15, 16, 17, 22, 23, and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Renner et al., US Patent 4,75,544.

3. Referring to claim 1, Renner et al. have taught a digital signal processor comprising:

a. a programmable, multiply and accumulate mathematical processor (Figure 1, Figure 5, element 24);

b. an input processor that processes input signals to the digital signal processor (Figure 1, element 12);

c. an output processor that processes output signals from the digital signal processor (Figure 1, element 20a);

d. a master processor that controls said mathematical processor, said input processor and said output processor (Figure 1, element 10, column 3, lines 13-20); and

e. a storage selectively accessible by each of the processors (column 3, lines 23-26, External ROM).

4. Referring to claim 2, Renner et al. have taught the digital signal processor of claim 1 further including a random access memory processor that stores intermediate calculation results (Figure 1, element 20b, Figure 4, element 202).

5. Referring to claim 3, Renner et al. have taught the digital signal processor of claim 2 including a bus coupling each of said processors to said storage (column 3, lines 23-26, External ROM, column 3, lines 13-20).

6. Referring to claim 4, Renner et al. have taught the digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations (Figure 3, element 12 implements many mathematical operations, such as elements 162, 158, 154. Figure 4, element 20a implements many mathematical operations, such as elements 212, 210, 208, 196, 190).

7. Referring to claim 5, Renner et al. have taught the digital signal processor of claim 1 wherein each of said processors have their own instruction sets (abstract).

8. Referring to claim 6, Renner et al. have taught the digital signal processor of claim 1 wherein said processors communicate with one another through said storage (column 3, lines 23-26, External ROM, Communication of the processors is through the entire system, including the storage.).

9. Referring to claim 8, Renner et al. have taught the digital signal processor of claim 1 where said master processor provides the timing for the other processors (Figure 1, element 10, column 3, lines 13-25, The master processor determines the timing for when the processors execute instructions because it controls when the instructions are sent.).

10. Referring to claim 9, Renner et al. have taught the digital signal processor of claim 1 wherein said master processor waits for the input processor to complete a given operation (Inherent because this system is clocked.).

11. Referring to claim 10, Renner et al. have taught the digital signal processor of claim 1 wherein each of said processors includes its own random access memory (Figure 3, element 132, Figure 4, element 202, Figure 5, element 220, inherent in element 10).

12. Referring to claim 14, Renner et al. have taught the digital signal processor of claim 1 including a mathematical processor which is pipelined (column 14, lines 58-61).

13. Referring to claim 15, Renner et al. have taught the digital signal processor of claim1 wherein said mathematical processor is a multi-cycled mathematical processor (column 14, lines 58-61, where an operation takes multiple cycles to complete. In this case a pipelined processor takes multiple cycles to complete.).

14. Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

15. Claim 17 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

16. Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

17. Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renner et al., US Patent 4,75,544.

20. Referring to claim 7, Renner et al. have taught the digital signal processor of claim 1, as described above. Renner et al. have not specifically taught wherein each of said processors use very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for the processors of Renner et al. to be issued several instructions at once and ensured, by the nature of VLIW instructions, that the compiler would have only combined instructions that are not dependent upon one another. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the very long instruction word format for instructions issued to the plural processors of Renner et al. in order to increase speed and efficiency of those processors. Official notice has been taken.

21. Claims 11-13, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renner et al., US Patent 4,75,544, in view of Nakagawa et al., U.S. Patent Number 5,241,679 (hereinafter Nakagawa).

22. Referring to claim 11, Renner et al. have not taught the digital signal processor wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register. Nakagawa has taught a storage including a plurality of registers (Nakagawa figure 1), where the registers automatically transfer existing data from a first register to a second register when new data is written into the first register (Nakagawa column 4, line 53 to column 5, line 16 and figure 2). Replacing the storage of Renner et al. with the multi-register storage of Nakagawa would

have allowed for the contents of all the registers to be saved, in case of an interrupt or context switch, simultaneously to the dedicated stack memories in order to perform both saving and restoration at a high speed (Nakagawa column 2, lines 17-23 and 42-49). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the multi-register storage system of Nakagawa instead of the generic storage means in the system of Renner et al. in order to increase the speed at which context preserving and restoration occurs.

23. Referring to claim 12, Nakagawa has taught the digital signal processor wherein said input processor causes the automatic transfer of data (Nakagawa column 4, line 53 to column 5, line 16 where the processor causing the data to be stored is necessarily an input processor).

24. Referring to claim 13, Nakagawa has taught the digital signal processor wherein the mathematical processor causes said data to be transferred from one register to another (Nakagawa column 4, line 53 to column 5, line 16).

25. Claims 18-20 do not recite limitations above the claimed invention set forth in claims 11-13 and are therefore rejected for the same reasons set forth in the rejection of claims 11-13 above.

26. Referring to claim 21, Nakagawa has taught storing a bit which indicates which processor may controls aid automatic transfer of data from one register to another (Nakagawa column 2, lines 29-33).

Response to Arguments

27. Applicant's arguments with respect to claims1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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